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APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

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METHOD AND APPARATUS FOR ADJUSTING tOH TIMING OF AN OUTPUT CIRCUIT

Field of the Invention

The present invention relates to method and apparatus for adjusting the timing of data availability at an output buffer of a digital circuit and more particularly to a method and apparatus for individually adjusting the data hold timing of each output buffer circuit for a multi-bit data path.

Background of the Invention

FIG. 1 illustrates a conventional output circuit for a digital circuit. To simplify discussion, this application will assume that the digital circuit is a memory circuit; however, it should be understood that the invention described herein applies to any circuit which outputs data. Data lines 11a, 11b...11n each receive a respective data bit DQ0, DQ1...DQn from a memory core, and provide the respective data bits to respective output buffer latches 13a, 13b...13n which in turn deliver the latched output data DQ0, DQ1...DQn to a plurality of output data lines 15a, 15b...15n. The output buffer latches 13a, 13b...13n are clocked by a clock signal which originates from a clock source 17 and is provided to the output buffer latches 13a, 13b...13n in common, either directly from clock source 17, or through a delay circuit 19. The clock signal applied to the output buffer latches 13a, 13b...13n causes the output buffers to

latch in data from the data lines 11a, 11b...11n and make it available on the output lines 15a, 15b...15n for a period of time know as the data hold time, commonly referred to as t_{oh}.

As shown in FIG. 2 a first clock cycle is used to synchronize a READ operation which causes the data DQ0, DQ1...DQn to be delivered from a memory core to the lines 11a, 11b...11n and a subsequent clock cycle T_1 causes the output buffers to latch and hold the data on lines 11a, 11b...11n for the data hold time. The time the data DQ0, DQ1...DQn is accessed from memory locations and during which it is made available on lines 11a, 11b...11n is commonly referred to as memory access time, t_{ac}.

Referring back to FIG. 1, a delay circuit 19 is often employed to ensure that data is available on all of the data input lines 11a, 11b...11n before the output buffers latch and hold the data.

As the speed of digital circuits continues to increase there are ever increasing demands placed on the timing circuitry for memory devices due to shorter clock periods. In addition, the very complex circuitry of modern digital circuits, e.g., memory devices, often leads to clock signal lines being routed to the output buffer latches 13, 13b...13n with unequal circuit path lengths both inside a chip and/or outside a chip in the chip packaging. As a consequence of these signal path length differences, and other timing aberrations caused by circuit topology within a chip, at

higher clocking speeds, it is becoming increasingly difficult to time align the data across all the output lines 15a, 15b...15c of a memory device.

SUMMARY OF THE INVENTION

The present invention is directed to a data output circuit for digital circuits, for example, memory circuits, which insures that the output data signals DQ0, DQ1...DQn applied to respective data output lines are delivered in substantial coincidence. This is accomplished by individually adjusting the clock signal applied to each of a plurality of output buffer latch circuits 13a, 13b...13n so that the timing of the delivery of the output signals on the output lines can be fine tuned to be substantially coincident, regardless of clock path length differences within a chip and/or within the leads of a chip package.

The invention can also be used to individually adjust the clock signals to respective output buffer circuits to deliver the output data signal DQ0, DQ1...DQn to respective output data lines such that the data signals arrive substantially coincidentally at the output terminals of a packaged digital circuit, for example, a memory circuit.

The invention employs respective adjustable delay circuits in the clock path from a clock source to each of the output buffer latches so that the data hold time tOH for each output buffer latch can be individually adjusted. The amount of delay for each adjustable delay circuit may be programmable .

These and other features and advantages of the invention will be better understood from the following detailed description which is provided in connection with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a conventional data output circuit;

FIG. 2 illustrates a timing diagram showing operation of the FIG. 1 data output circuit;

FIG. 3 illustrates a data output circuit constructed in accordance with of the invention;

FIG. 4 illustrates the delay control circuit depicted in FIG. 3; and

FIG. 5 illustrates a processor based system which may employ the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 3 illustrates an embodiment of a data output circuit of the invention. Like elements to those in FIG. 1 have the same reference numbers. The FIG. 3 data output circuit permits the data hold time of the output buffer latches 13a, 13b...13n to

be individually adjusted by means of a respective delay control circuits 21a, 21b...21n, each of which delivers a clock signal from a clock source 17 to a respective output buffer latch 13. The delay control circuits 21a, 21b...21n each provide an individually adjustable delay so that the timing of the clock signals delivered from clock source 17 to the respective output buffer latch circuits 13a, 13b...13n can be individually adjusted.

FIG. 4 illustrates an exemplary embodiment of one delay control circuit 21a. It should be understood that each of the delay control circuits 21b...21n in FIG. 3 have an identical construction. Each delay control circuit includes a switch circuit for selecting one of a plurality of delay elements to be used to delay an applied clock signal. The switch circuit is shown in FIG. 4 as a plurality of switch element 23a, 23b...23m. Each switch element 23a, 23b...23m receives the incoming clock signal and is in turn connected to a respective delay element 25a, 25b...25m. The delay elements are each capable of applying a different predetermined delay with respect to an input signal applied thereto. For example, delay element 25a may deliver a .5 nanosecond delay, delay element 25b a 1.0 nanosecond delay and delay element 25m a 1.5 nanosecond delay. It should be apparent from FIG. 4 that although three switch elements 23a, 23b...23m and three associated delay elements 25a, 25b...25m are illustrated that any number of switch elements and delay elements may be used. It should also be apparent that many different types of switch circuits could be used to select one of the delay elements 25a, 25b...25m for delaying the applied clock signal.

As noted, the switch elements 23a, 23b...23m all act as switches and the "on" state of each switch element is controlled by a signal which is applied to it through a respective fuse element or anti-fuse element, 27a, 27b...27m. In practice, one of the fuse or anti-fuse elements 27a, 27b...27m will be "set" relative to the others so that one of the switch elements 23a, 23b...23m is "on" while the rest remain "off." As a consequence, the arriving clock signal DQCLK from clock source 17 which commonly enters each of the switch elements 23a, 23b...23m is passed by the "on" switch to its corresponding delay element 25a, 25b...25m thereby delivering a delayed clock signal DQCLKD to a respective output buffer 13a. The delay control circuit 21a illustrated in FIG. 4 can accordingly be programmed with the fuses or anti-fuses to set a particular clock signal delay for a particular output buffer as desired. The fused or anti-fused devices 27a, 27b...27c can be programmed by the manufacturer, or by a user. If the fuses or anti-fuses are programmed by a manufacturer, the fuses or anti-fuses can be programmed during fabrication and before chip packaging. Alternatively, external pins may be provided on the chip for programming the fuses or anti-fuses by a user.

Returning to the timing diagram of FIG. 2, the delay control circuitry 21a of the invention thus enables the data output circuit of a digital circuit, e.g., a memory circuit, to individually adjust the data hold time of each output buffer to best accommodate the clock signal path characteristics of the digital circuit and/or its packaging. As a result, the data hold times of all output buffers can be made

substantially coincident, either at the output of the buffers or at the output terminals of the digital circuit.

The invention may be easily implemented as part of a digital integrated circuit. The present invention will find particular utility in a digital circuit which uses output buffers to apply data signals to a transmission path, such as a data bus, such as digital circuits employed in a processor based system of the type illustrated in FIG. 5.

As shown in FIG. 5, a processor based system, such as a computer system, generally comprises a central processing unit (CPU) 210, for example, a microprocessor, which communicates with one or more input/output (I/O) devices 240, 250 over a bus 270. The system 200 may also includes random access memory (RAM) 260, a read only memory (ROM) 280 and may include other peripheral devices such as a floppy disk drive 220 and a compact disk (CD) ROM drive 230 which also communicate with CPU 210 over the bus 270. At least one of CPU 210 and one or more integrated circuits connected thereto, such as employed for RAM 260 and ROM 280, may contain the data output circuit described above with reference to FIGS. 3 and 4. It is also possible to integrate the processor 210 and one or more of RAM 260 and ROM 280 on a single IC chip. FIG. 5 is one exemplary processor based architecture with which the invention may be used. Many other processor based architectures are also possible.

While a preferred embodiment of the invention has been described and illustrated above, it should be understood that this is exemplary of the invention and are not to be considered as limiting. Additions, deletions, substitutions, and other modifications can be made without departing from the spirit or scope of the present invention. Accordingly, the invention is not to be considered as limited by the foregoing description, but is only limited by the scope of the appended claims.